CLAIMS

What is claimed is:

1. In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:

loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of an aligned vector to be generated;

loading a second vector from the memory unit into a second register;

determining a starting byte in the first register wherein the starting byte specifies the first byte of an aligned vector;

extracting a first width vector from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register; and

replicating the extracted first width vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.

2. The method as recited in Claim 1 further comprising the step of storing the aligned vector in the third register to the memory unit.

3. The method as recited in Claim 1, wherein the first width and second width are each 64 bits.

4. The method as recited in Claim 3, wherein the third register is comprised of 8 8-bit elements.

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5. The method as recited in Claim 3, wherein the third register is comprised of 4 16-bit elements.

6. The method as recited in Claim 1, wherein the starting byte is specified as a constant in an alignment instruction.

7. The method as recited in Claim 1, wherein the starting byte is specified as a variable in a register in an alignment instruction.

8. The method as recited in Claim 1, wherein the first vector and the second vector are in contiguous location in the memory unit.

9. The method as recited in Claim 1, wherein the processor operates in a big-endian byte ordering mode.

10. The method as recited in Claim 1, wherein the processor operates in a little-endian byte ordering mode.

11. In a computer system including a processor having a plurality of registers, a method for generating an ordered set of elements in an N-bit vector from two sets of elements in two N-bit vectors for single instruction multiple data (SIMD) vector processing, said method comprising the steps of:

loading a first vector from a memory unit into a first register;

loading a second vector from the memory unit into a second register;

selecting a subset of elements from the first register and the second register; and

replicating the elements from the subset into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

12. The method as recited in Claim 11 further comprising the step of storing the elements in the third register to the memory unit.

13. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 4 16-bit elements indexed from 0 to 3.

14. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 8 8-bit elements indexed from 0 to 7.

15. The method as recited in Claim 13, wherein the subset is comprised of two elements from the first register and two elements from the second register.

16. The method as recited in Claim 14, wherein the subset is comprised of four elements from the first register and four elements from the second register.

17. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2 and 3 from the second register.

18. The method as recited in Claim 17, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;

the element 1 replicated from the element 2 of the first register;

the element 2 replicated from the element 3 of the second register; and

the element 3 replicated from the element 3 of the first register.

19. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 1 from the first register and the elements 0 and 1 from the second register.

20. The method as recited in Claim 19, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 0 of the first register;

the element 2 replicated from the element 1 of the second register; and

the element 3 replicated from the element 1 of the first register.

21. The method as recited in Claim 13, wherein the subset is comprised of the elements 1 and 3 from the first register and the elements 1 and 3 from the second register.

22. The method as recited in Claim 21, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;

the element 1 replicated from the element 3 of the second register;

the element 2 replicated from the element 1 of the first register; and

the element 3 replicated from the element 3 of the first register.

23. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0 and 2 from the second register.

24. The method as recited in Claim 23, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 2 of the second register;

the element 2 replicated from the element 0 of the first register; and

the element 3 replicated from the element 2 of the first register.

25. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1 and 3 from the second register.

26. The method as recited in Claim 25, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;

the element 1 replicated from the element 0 of the first register;

the element 2 replicated from the element 3 of the second register; and

the element 3 replicated from the element 2 of the first register.

27. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1 and 3 from the second register.

28. The method as recited in Claim 27, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 3 of the second register;

the element 1 replicated from the element 2 of the first register;

the element 2 replicated from the element 1 of the second register; and

the element 3 replicated from the element 0 of the first register.

29. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2 and 3 from the second register.

30. The method as recited in Claim 29, wherein particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;

the element 1 replicated from the element 3 of the second register;

the element 2 replicated from the element 2 of the first register; and

the element 3 replicated from the element 3 of the first register.

31. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0 and 1 from the second register.

32. The method as recited in Claim 31, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 1 of the second register;

the element 2 replicated from the element 0 of the first register; and

the element 3 replicated from the element 2 of the first register.

33. The method as recited in Claim 14, wherein the subset is comprised of the elements 1, 3, 5, and 7 from the first register and the elements 1, 3, 5, and 7 from the second register.

34. The method as recited in Claim 33, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;

the element 1 replicated from the element 3 of the second register;

the element 2 replicated from the element 5 of the second register;

the element 3 replicated from the element 7 of the second register;

the element 4 replicated from the element 1 of the first register;

the element 5 replicated from the element 3 of the first register;

the element 6 replicated from the element 5 of the first register; and

the element 7 replicated from the element 7 of the first register.

35. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 2, 4, and 6 from the first register and the elements 0, 2, 4, and 6 from the second register.

36. The method as recited in Claim 35, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 2 of the second register;

the element 2 replicated from the element 4 of the second register;

the element 3 replicated from the element 6 of the second register;

the element 4 replicated from the element 0 of the first register;

the element 5 replicated from the element 2 of the first register;

the element 6 replicated from the element 4 of the first register; and

the element 7 replicated from the element 6 of the first register.

37. The method as recited in Claim 14, wherein the subset is comprised of the elements 4, 5, 6, and 7 from the first register and the elements 4, 5, 6, and 7 from the second register.

38. The method as recited in Claim 37, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 4 of the second register;

the element 1 replicated from the element 4 of the first register;

the element 2 replicated from the element 5 of the second register;

the element 3 replicated from the element 5 of the first register;

the element 4 replicated from the element 6 of the second register;

the element 5 replicated from the element 6 of the first register;

the element 6 replicated from the element 7 of the second register; and

the element 7 replicated from the element 7 of the first register.

39. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 1, 2, and 3 from the first register and the elements 0, 1, 2, and 3 from the second register.

40. The method as recited in Claim 39, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 0 of the first register;

the element 2 replicated from the element 1 of the second register;

the element 3 replicated from the element 1 of the first register;

the element 4 replicated from the element 2 of the second register;

the element 5 replicated from the element 2 of the first register;

the element 6 replicated from the element 3 of the second register; and

the element 7 replicated from the element 3 of the first register.

41. The method as recited in Claim 14, wherein the subset is comprised of the elements 4, 5, 6, and 7 from the first register.

42. The method as recited in Claim 41, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 4 of the first register;

the element 2 replicated from the element 5 of the first register;

the element 4 replicated from the element 6 of the first register;

the element 6 replicated from the element 7 of the first register; and

the elements 1, 3, 5, and 7 containing a zero in all the bits.

43. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 1, 2, and 3 from the first register.

44. The method as recited in Claim 43, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the first register;

the element 2 replicated from the element 1 of the first register;

the element 4 replicated from the element 2 of the first register;

the element 6 replicated from the element 3 of the first register; and

the elements 1, 3, 5, and 7 containing a zero in all the bits.

45. The method as recited in Claim 14, wherein the subset is comprised of the elements 4, 5, 6, and 7 from the first register.

46. The method as recited in Claim 45, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 4 of the first register;

the element 1 replicating the sign bit of the element 4 of the first register in all the bits;

the element 2 replicated from the element 5 of the first register;

the element 3 replicating the sign bit of the element 5 of the first register in all the bits;

the element 4 replicated from the element 6 of the first register;

the element 5 containing the sign bit of the element 6 of the first register in all the bits;

the element 6 replicated from the element 7 of the first register; and

the element 7 containing the sign bit of the element 7 of the first register in all the bits.

47. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 1, 2, and 3 from the first register.

48. The method as recited in Claim 47, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the first register;

the element 1 containing the sign bits of the element 0 of the first register;

the element 2 replicated from the element 1 of the first register;

the element 3 containing the sign bits of the element 1 of the first register;

the element 4 replicated from the element 2 of the first register;

the element 5 containing the sign bits of the element 2 of the first register;

the element 6 replicated from the element 3 of the first register; and

the element 7 containing the sign bits of the element 3 of the first register.

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